Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (currently amended). A device to synthesize a range of frequencies F1-F2 with high spectral purity, comprising:

a variable-step synthesizer <u>Na</u> providing a range of frequencies F3-F4[[, Na]];

a variable ratio divider Nb <u>connected to said variable step-synthesizer for receiving the range of frequencies from said variable-step synthesizer;</u> and

a frequency control device adapted for delivering a division rank command of the variable ratio divider, a command of the frequency of the variable-step synthesizer, and a command of a synthesis step of the variable-step synthesizer <u>and connected at one output to said variable-step frequency synthesizer and at another output to said variable ratio divider,</u>

wherein <u>a</u> [[the]] length of the cycle of evolution of Na is variable and dependent on the value of Nb, the variable-step synthesizer is a fractional step phase-locked loop synthesizer.

2. (previously presented). The device according to claim 1 comprising a filtering device positioned after the variable ratio divider Nb.

Claim 3 (cancelled).

4. (currently amended). The device according to claim 1 wherein the variable ratio divider Nb is a value from N1 to Np, the values N1 to Np follow an arithmetic progression, and wherein <u>a</u> [[the]] maximum frequency of the synthesizer is given by F4=N1*F2 where N1 is the smallest value of the sequence of values N1 to Np and the frequency F3 is a function of N2.

5. (previously presented). The device according to claim 4 wherein the value of the

frequency F3 is substantially equal to or slightly lower than (N1/N2)*F4.

6. (previously presented). The device according to claim 1 wherein the variable ratio divider Nb is a value from N1 to Np, the values N1 to Np following a non-arithmetic progression.

7. (previously presented). The device according to claim 6 wherein F3 is substantially equal to or smaller than a F4 where a is the smallest value obtained in dividing two consecutive values one after the other.

8. (previously presented). The device according to claim 6 wherein the highest division rank Nb is chosen.

9. (currently amended). The device according to claim 1 <u>further</u> comprising a mixer receiving an output signal from <u>the variable</u> a̶ ̶f̶r̶a̶c̶t̶i̶o̶n̶a̶l̶ step synthesizer and a mixing signal.

10. (currently amended). A method of synthesizing a range of frequencies F1-F2 with high spectral purity u̶s̶i̶n̶g̶ ̶a̶ ̶v̶o̶l̶t̶a̶g̶e̶ ̶c̶o̶n̶t̶r̶o̶l̶l̶e̶d̶ ̶o̶s̶c̶i̶l̶l̶a̶t̶o̶r̶, a frequency source which comprises the steps of:

dividing the output signal of <u>a</u> [[the]] voltage controlled oscillator by a first value Nb, and;

dividing <u>an</u> [[the]] input signal of the voltage controlled by a second value Na,

wherein <u>a</u> [[the]] length of the cycle of evolution of Na is variable and dependent on <u>a</u> [[the]] value of Nb.

11. (currently amended). The method according to claim 10 wherein <u>a</u> [[the]] value of Nb varies according to an arithmetic sequence N1...Np and wherein <u>a</u> [[the]] frequency F4 is determined by N1*F2 and <u>a</u> [[the]] frequency F3 is a function of N2.

12. (currently amended). The method according to claim 11 wherein <u>a</u> [[the]] value of the frequency F3 is chosen to be substantially equal to or slightly below (N1/N2)*F4.

13. (currently amended). The method according to claim 10 wherein a [[the]] value of Nb varies according to a non-arithmetic sequence and wherein two consecutive values of the sequence are divided.

14. (previously presented). The method according to claim 13 wherein F3 is substantially equal to or smaller than a F4 where a is the smallest value obtained in dividing two consecutive values of the sequence.

15. (previously presented). The method according to claim 14 wherein the highest division rank Nb is chosen.

16. (previously presented). The method according to claim 10, wherein the modification of the division rank and the synthesis step is simultaneous.

17. (previously presented). The method according to claim 1, wherein a ratio of a reference frequency to the frequency step, is a least common multiple of the sequence N1...Np.

18. (original) The device according to claim 1 wherein reference frequency Fref is chosen so that the desired fractional step values are obtained.

19. (original) The method according to claim 10 wherein the reference frequency Fref is chosen so that the desired fractional step values are obtained as Fref is a function of sequence of the values N1, N2, ... Np assumed by Nb.

20. (original) The method according to claim 10 wherein the reference frequency Fref is chosen so that the desired fractional step values are obtained as follows Fref/ΔF must be a multiple of the LCM of N1, N2, ... Np with ΔF a given frequency step.